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L8: Entry 1 of 4

File: PGPB

Nov 14, 2002

PGPUB-DOCUMENT-NUMBER: 20020169945

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020169945 A1

TITLE: Microprocessor

PUBLICATION-DATE: November 14, 2002

INVENTOR-INFORMATION:

NAME CITY STATE COUNTRY RULE-47

Haraguchi, Yoshiyuki Tokyo JP

US-CL-CURRENT: 712/205; 712/234, 712/241

Full Title Citation Front Review Classification Date Reference Sequences Attachments Claims KMC Draw. De

☐ 2. Document ID: US 20020083312 A1

L8: Entry 2 of 4

File: PGPB Jun 27, 2002

PGPUB-DOCUMENT-NUMBER: 20020083312

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020083312 A1

TITLE: Branch Prediction apparatus and process for restoring replaced branch

history for use in future branch predictions for an executing program

PUBLICATION-DATE: June 27, 2002

INVENTOR-INFORMATION:

NAME CITY STATE COUNTRY RULE-47

Sinharoy, Balaram Poughkeepsie NY US

US-CL-CURRENT: 712/240

Full Title Citation Front Review Classification Date Reference Sequences Attachments Claims KWC Draw De

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☐ 3. Document ID: US 6745320 B1

L8: Entry 3 of 4

File: USPT

Jun 1, 2004

US-PAT-NO: 6745320

DOCUMENT-IDENTIFIER: US 6745320 B1

TITLE: Data processing apparatus

Full Title Citation Front Review Classification Date Reference Claims Claims KMC Draw De

1. Document ID: US 5333280 A

1. L8: Entry 4 of 4 File: USPT Jul 26, 1994

US-PAT-NO: 5333280

DOCUMENT-IDENTIFIER: US 5333280 A

TITLE: Parallel pipelined instruction processing system for very long instruction

word

Full	Title	Citation	Front	Review	Classification	Date	Reference		11.7		Claims	KWMC	Draw De
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	(L7	AND L	.2).PG	PB,US	PT,USOC,I	EPAB	,JPAB,E	WPI,TI	OBD.			4	

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L13: Entry 1 of 10

File: USPT

Jun 1, 2004

US-PAT-NO: 6745320

DOCUMENT-IDENTIFIER: US 6745320 B1

TITLE: Data processing apparatus

DATE-ISSUED: June 1, 2004

INVENTOR-INFORMATION:

NAME

CITY

STATE

ZIP CODE

COUNTRY

Mitsuishi; Naoki

Kodaira

JP

US-CL-CURRENT: 712/225; 711/212, 711/214, 712/201, 712/202, 712/203, 712/209,

712/227, 712/245

1	Full	Title	Citation	Front	Review	Classification	Date	Reference	a seed appears exhibited that	Cla	ims	OMC	Drawi De
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	L13	3: En	try 2 c	of 10			File:	USPT		May	18,	200	14

US-PAT-NO: 6738893

DOCUMENT-IDENTIFIER: US 6738893 B1

TITLE: Method and apparatus for scheduling to reduce space and increase speed of microprocessor operations

Full	Title	Citation	Front	Review	Classification	Date	Reference	SERVICES MILENDEDS	Claims	KOMO	Drawi De
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	3. I	Oocume	nt ID:	US 66	15339 B1						
L13	: Ent	ry 3 c	of 10			File	: USPT		Sep 2	. 200)3

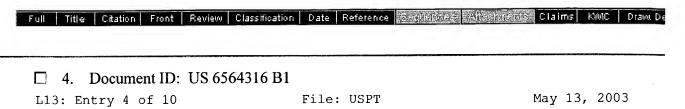
US-PAT-NO: 6615339

DOCUMENT-IDENTIFIER: US 6615339 B1

TITLE: VLIW processor accepting branching to any instruction in an instruction word

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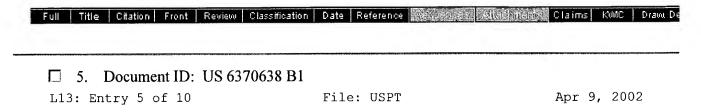
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US-PAT-NO: 6564316

DOCUMENT-IDENTIFIER: US 6564316 B1

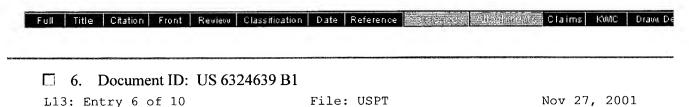
TITLE: Method and apparatus for reducing code size by executing no operation instructions that are not explicitly included in code using programmable delay slots



US-PAT-NO: 6370638

DOCUMENT-IDENTIFIER: US 6370638 B1

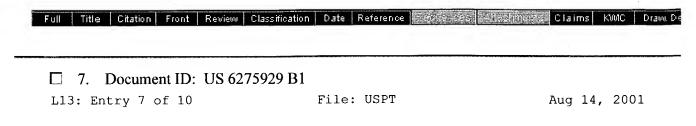
TITLE: Apparatus and method of computer program control in computer systems using pipeline processing



US-PAT-NO: 6324639

DOCUMENT-IDENTIFIER: US 6324639 B1

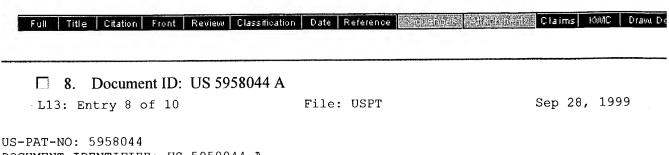
TITLE: Instruction converting apparatus using parallel execution code



US-PAT-NO: 6275929

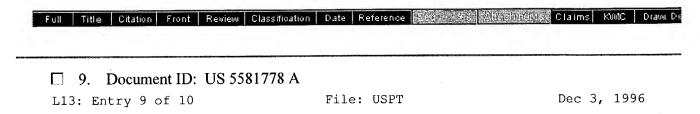
DOCUMENT-IDENTIFIER: US 6275929 B1

TITLE: Delay-slot control mechanism for microprocessors



DOCUMENT-IDENTIFIER: US 5958044 A

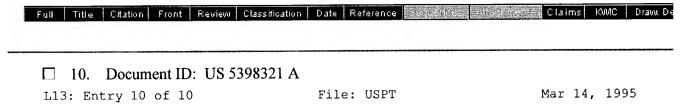
TITLE: Multicycle NOP



US-PAT-NO: 5581778

DOCUMENT-IDENTIFIER: US 5581778 A

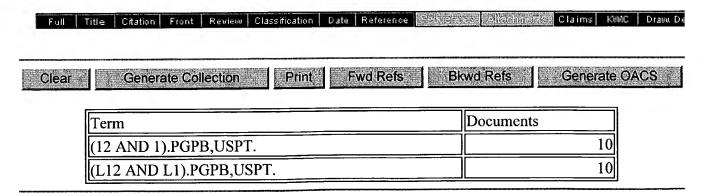
TITLE: Advanced massively parallel computer using a field of the instruction to selectively enable the profiling counter to increase its value in response to the system clock



US-PAT-NO: 5398321

DOCUMENT-IDENTIFIER: US 5398321 A

TITLE: Microcode generation for a scalable compound instruction set machine



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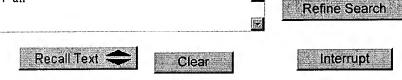
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<u>L8</u> L7 and 12	4	<u>L8</u>
<u>L7</u> L6 and 11	16	<u>L7</u>

<u>L6</u>	(end or last or least) near8 branch\$3 near5 (portion\$1 or field\$1)	9690	<u>L6</u>
<u>L5</u>	L4 and l2	57	<u>L5</u>
<u>L4</u>	(NOP or (("no" or iddle) near2 operation\$1)) near15 (branch or conditional or instruction) near5 (field\$1 or portion\$1)	218	<u>L4</u>
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<u>L3</u>	L2 and 11	70	<u>L3</u>
<u>L2</u>	(712/221-300)![CCLS]	4658	<u>L2</u>
DB=	PGPB, USPT, USOC, EPAB, JPAB, DWPI, TDBD; PLUR=YES; OP=OR		
<u>L1</u>	(NOP or (("no" or iddle) near2 operation\$1)) near15 (branch or conditional or instruction) near5 (field\$1 or portion\$1 or format)	256	<u>L1</u>

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